

1/1 IDS 7/21/03

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2357		priority SERIAL NO. 10/364,054	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
				priority FILING DATE February 10, 2003		priority GROUP 2812	

10/624716

U.S. PATENT DOCUMENTS								
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
<div style="display: flex; flex-direction: column; align-items: center;"> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> <div>QU</div> </div>	AA	6,458,666 B2	10-2002	Wasshuber			/	
	AB	6,444,548 B2	09-2002	Divakaruni et al.				
	AC	3,886,003	05-1975	Takagi et al.				
	AD	4,366,338	12-1982	Turner et al.				
	AE	6,008,115	12-1999	Jung				
	AF	6,506,647 B2	01-2003	Kuroda et al.				
	AG	US2001/0036713A1	11-01-2001	Rodder et al.				July 5, 2001
	AH	US2002/0034865A1	03-21-2002	Umimoto et al.				Nov. 30, 2001
	AI	09/876,722		Scott				June 6, 2001
	AJ	10/133,193		McQueen et al.				April 26, 2002
AK								
AL								

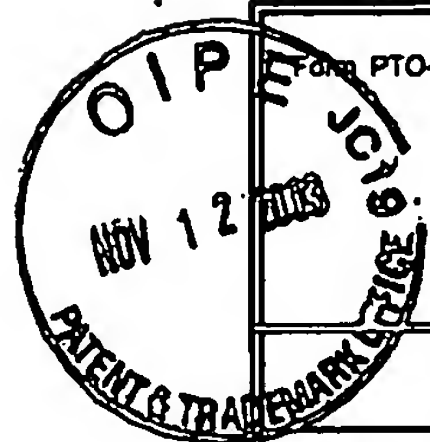
FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
<div style="display: flex; flex-direction: column; align-items: center;"> <div>QU</div> <div>QU</div> <div>QU</div> </div>	AQ		Young et al., "A 0.13 μ m CMOS Technology with 193 nm Lithography and Cu/Low-k for High Performance Applications", IEDM, pgs. 563-566, April 2000.
<div style="display: flex; flex-direction: column; align-items: center;"> <div>QU</div> </div>	AR		Yeh et al., "Optimum Halo Structure for Sub-0.1 μ m CMOSFETs", IEEE Transactions on Electronic Devices, Vol. 48, No. 10, October 2001, pgs. 2357-2362.
<div style="display: flex; flex-direction: column; align-items: center;"> <div>QU</div> </div>	AS		Bouillon et al., "Re-examination of Indium implantation for a low power 0.1 μ m technology", IDEM, pgs. 897-900, 1995 (year is sufficient so that date is not in issue).

EXAMINER <div style="font-size: 1.5em; font-family: cursive;">James M. Kennedy</div>	DATE CONSIDERED <div style="font-size: 1.5em; font-family: cursive;">Feb 15, 2005</div>
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1/3 IDS 11/12/03



Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2357		SERIAL NO. 10/624,716		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran		FILING DATE July 21, 2003		
				GROUP 2812				
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
JK	AA	6,144,079 A	11-2000	Shirahata et al.				
JK	AB	6,033,952	03-2000	Yasumura, et al.				
JK	AC	6,124,168	09-2000	Ong				
JK	AD	5,688,705	11-1997	Bergemont				
JK	AE	5,866,448	02-1999	Pradeep et al.				
JK	AF	5,858,847	01-1999	Zhou et al.				
JK	AG	6,380,598	04-2002	Chan				
JK	AH	6,060,364	05-2000	Maszara et al.				
JK	AI	6,194,276 B1	02-2001	Chan et al.				
JK	AJ	6,359,319 B1	03-2002	Noda				
JK	AK	5,164,806	11-1992	Nagatomo et al.				
JK	AL	4,937,756	06-1990	Hsu et al.				
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes No	
JK	AM	EP 0718881	06/96	EPO, Chan				
	AN							
	AO							
	AP							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
JK	AR		Watanabe, H. et al., Novel 0.44µm ² Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application, IEEE 1998, pp. 36.2.1 - 36.2.4.					
JK	AS		Wolf, S., "Silicon Processing for the VLSI Era", Vol. 2, pp. 632-635.					
JK	AT		MITSUBISHI ELECTRIC WEBSITE: Reprinted from website http://www.mitsubishielectric.com/r_and_d/tech_showcase/ts8.php on 3/29/2001: "8. Production Line Application of a Fine Hole Pattern-Formation Technology for Semiconductors", on 3/29/2001, 4 pgs					
EXAMINER		Jennifer M. Kennedy			DATE CONSIDERED			Feb. 15, 2005
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Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-2357SERIAL NO.
10/624.716LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Luan C. TranFILING DATE
July 21, 2003GROUP
2812

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Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
QU	AA	5,930,614	07-1999	Eimori et al.			
QU	AB	5,635,744	06-1997	Hidaka et al.			
QU	AC	6,204,536	03-2001	Maeda et al.			
QU	AD	6,515,899 B1	02-2003	Tu et al.			
QU	AE	4,570,331	02-1986	Eaton, Jr. et al.			
QU	AF	6,429,079 B1	08-2002	Maeda et al.			
QU	AG	6,607,979 B1	08-2003	Kamiyama			
QU	AH	4,686,000	08-1987	Heath			
QU	AI	5,814,875	09-1998	Kumazaki			
QU	AJ	5,654,573	08-1997	Oashi et al.			
QU	AK	6,479,330 B2	11-2002	Iwamatsu et al.			
QU	AL	6,586,803	07-2003	Hidaka et al.			

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

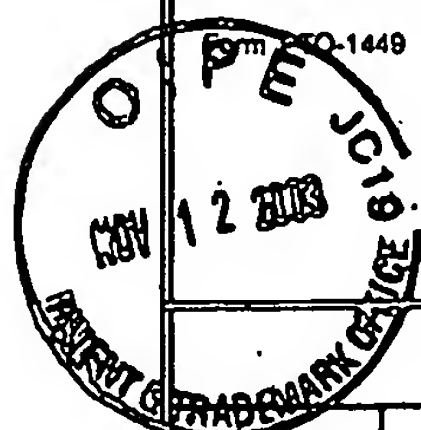
QU	AR		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/issues/1999/sep99/docs/feature1.asp on 3/29/2001: "Resists Join the Sub-A Revolution", 9 pgs.
QU	AS		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp on 3/29/2001: "Paths to Smaller Features", 1 pg.
QU	AT		Wolf, S., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press 1986, pp. 434-437.

EXAMINER

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				ATTY. DOCKET NO. M122-2357		SERIAL NO. 10/624.716		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran				
				FILING DATE July 21, 2003		GROUP 2812		
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
JA	AA	6,552,401 B1	04-2003	Dennison				
JA	AB	6,627,524 B2	09-2003	Scott				
JA	AC	US2002/0182829A1	12-2002	Chen				
JA	AD	US2002/0164846A1	11-2002	Lin et al.			Apr. 19, 2002	
JA	AE	US2003/0071310A1	04-2003	Salling et al.			Oct. 11, 2001	
	AF							
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FOREIGN PATENT DOCUMENTS								
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
JA	AR		"Session 18: Integrated Circuits and Manufacturing - DRAM and Embedded DRAM Technology," 2001 IEDM Technical Program, 2001 IEEE International Electron Devices Meeting, Dec. 4, 2001, reprinted 11/15/01 from http://www.his.com/~iedm/techprogram/sessions/s18.html , pp. 1-2.					
	AS							
	AT							
EXAMINER		JENNIFER M. KENNEDY						
DATE CONSIDERED		Feb 13 2005						
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MAR-10-2004 13:49

WELLS ST. JOHN, P.S.

5098383424 P.03/03

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
M122-2357SERIAL NO.
10024716LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Luan C. TranFILING DATE
July 21, 2003GROUP
2511

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
QU	AA	6,521,487 B1	02-2003	Chen et al.			
QU	AB	6,492,694 B2	12-2002	Nohle et al.			
QU	AC	6,468,865 B1	10-2002	Yang et al.			
QU	AD	6,451,704 B1	09-2002	Pradeep et al.			
QU	AE	6,436,747 B1	08-2002	Segawa et al.			
QU	AF	6,362,034 B1	03-2002	Sandford et al.			
QU	AG	6,277,720 B1	08-2001	Umhi et al.			
QU	AH	5,923,975	07-1999	Rolandt			
QU	AI	5,866,934	02-1999	Kulush et al.			
QU	AJ	5,180,468 B1	01-2001	Yu et al.			
QU	AK	6,207,510 B1	03-2001	Abdin et al.			
QU	AL	US2003/0112012A1	02-2003	Wada et al.			

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		Document Number	Date	Country	Class	Subclass	Translation	
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER

Jennifer M. Kennedy

DATE CONSIDERED

Feb 13, 2005

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WELLS ST. JOHN, P. S.

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P.03/03

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. N022-2357		SERIAL NO. 10624716	
LIST OF ART CITED BY APPLICANT (If no answer, check (if necessary))				APPLICANT Luan C. Tran		FILING DATE July 21, 2003	
				GROUP 2B1			
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
JH JH JH	AA	5,841,185	11-1998	Ishikawa			
	AB	6,331,458 B1	12-2001	Anjum et al.			
	AC	6,251,744 B1	06-2001	Su et al.			
	AD						
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EXAMINER		DATE CONSIDERED					
Jenny M. Kennedy		Feb 15 2005					
*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 2112; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

1/1 IDS 11/1/04

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WELLS ST. JOHN, P.S.

5098383424 P.03/03

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M22-2357		SERIAL NO. 10624.716	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Loan C. Tran			
				FILING DATE July 21, 2003		GROUP 2811	
U.S. PATENT DOCUMENTS							
*Examiner (Initial)	Class	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
JM	AA	5,767,557	06-1998	Kizilyan			
JM	AB	5,369,295	11-1994	Vinal			
JM	AC	5,597,917	03-1995	Mookhi			
JM	AD	5,873,724	04-1999	Iliukha			
JM	AE	5,672,526	09-1997	Kiramuro			
JM	AF	5,725,714	07-1993	Wakamiya et al.			
JM	AG	5,441,161	08-1995	Iwamatsu et al.			
JM	AH	5,355,012	10-1994	Yamaguchi et al.			
JM	AJ	5,836,226	01-1999	Wu			
JM	AJ	5,877,056	03-1999	Wu			
JM	AK	6,518,113 B1	10-2003	Buyonoki			
JM	AL	6,642,581 B2	11-2003	Matsumoto et al.			
JM	AM	6,297,082 B1	10-2001	Lin et al.			
JM	AN	US2002/0043692A1	04-2002	Maceda et al.			
JM	AO	US2003/0189231	10-2003	Covenger et al.			
FOREIGN PATENT DOCUMENTS							
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EXAMINER <i>Jennifer M. Kennedy</i>				DATE CONSIDERED <i>Feb 15 2005</i>			
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